CLAIMS

What is claimed is:

1. A field effect transistor (FET) comprising:

a fin formed on a dielectric surface;

a device gate along one side of said fin;

a back bias gate along an opposite side of said fin;

device gate dielectric along one first side between said device gate and said fin; and

back bias gate dielectric along said opposite side between said back bias gate and said fin; wherein said back bias gate dielectric differs from said device gate dielectric in at least one of material and thickness.

2. A FET as in claim 1, wherein said fin is a semiconductor fin selected from a group of materials consisting of silicon, germanium and silicon-germanium.

3. A FET as in claim 2, wherein said fin is a silicon fin.

4. A FET as in claim 1, wherein one of said device gate dielectric and said back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers.

5. A FET as in claim 1, wherein said back bias gate dielectric is thicker than said gate dielectric.

6. A FET as in claim 1, wherein each of said back bias gate dielectric and said gate dielectric is selected from a group of materials consisting of an oxide, an oxynitride and a high K dielectric.

7. A FET as in claim 1, wherein said gate and said back bias gate are a conductive material selected from a group of materials consisting of a metal, doped silicon, doped germanium, doped silicon germanium and a metal silicide.

8. A FET as in claim 3, wherein said dielectric surface is an oxide layer.

9. A FET as in claim 8, wherein said oxide layer is a buried oxide layer.

10. A FET as in claim 8, wherein said oxide layer is disposed on a nitride layer.

11. A FET as in claim 3, further comprising a dielectric pillar above said silicon fin.

12. A FET as in claim 11, wherein said dielectric pillar is a nitride pillar.

13. A FET as in claim 12, wherein said nitride pillar forms a cap between said device gate and said back bias gate.

14. An integrated circuit (IC) on a semiconductor on insulator (SOI) chip, said IC including a plurality of field effect transistors (FETs) disposed on an insulating layer, each of said FETs comprising:

a semiconductor fin formed on an insulating layer;

device gate dielectric along a first side of said semiconductor fin;

a device gate along said device gate dielectric;

back bias gate dielectric along an opposite of said semiconductor fin;

a back bias gate along said back bias gate dielectric; wherein said back bias gate dielectric differs from said device gate dielectric in at least one of material and thickness.

15. An IC as in claim 14, wherein said back bias gate dielectric is five times (5X) thicker than said gate dielectric.

16. An IC as in claim 14, wherein each of said back bias gate dielectric and said gate dielectric is selected from a group of materials consisting of an oxide, an oxynitride and a high K dielectric.

17. An IC as in claim 14, wherein one of said device gate dielectric and said back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers.

18. An IC as in claim 14, wherein said gate and said back bias gate are a conductive material selected from a group of materials consisting of a metal, doped silicon, doped germanium, doped silicon germanium and a metal silicide.

19. An IC as in claim 14, wherein said dielectric surface is an oxide layer.

20. An IC as in claim 19, wherein said oxide layer is a buried oxide layer.

21. An IC as in claim 19, wherein said oxide layer is disposed on a nitride layer.

22. An IC as in claim 14, each said FET further comprising a dielectric pillar above said semiconductor fin.

23. An IC as in claim 22, wherein said dielectric pillar is a nitride pillar.

24. An IC as in claim 23, wherein said nitride pillar forms a cap between said device gate and said back bias gate.

25. An IC as in claim 22, wherein said semiconductor is silicon.

26. A method of forming an integrated circuit (IC), said method comprising the steps of:

a) forming semiconductor fins on a silicon on insulator (SOI) wafer;

b) forming back bias gates along one side of each of said semiconductor fins, said back bias gates comprising back bias gate dielectric; and

c) forming device gates along an opposite side of each of said semiconductor fins; said device gates comprising gate dielectric with at least one of material and thickness being different from said back bias gate dielectric.

27. A method of forming an IC as in claim 26, wherein the semiconductor fin is a silicon fin and the step (a) of forming silicon fins comprises the steps of:

i) forming a pillar on a silicon layer;

ii) etching a portion of said silicon layer, a first side of said silicon fins being defined by removal of said portion;

iii) protecting said first side; and

iv) etching remaining portions of said silicon layer, a second side of said silicon fins being defined by removal of said portions, silicon fins remaining at said pillars a second.

28. A method of forming an IC as in claim 27, wherein the semiconductor fin is a silicon fin and the step (i) of forming pillars comprises the steps of:

A) forming a dielectric layer on said silicon layer;

B) forming a sacrificial layer on said dielectric layer;

C) removing portions of said dielectric layer and said sacrificial layer; and

D) forming said pillars alongside remaining portions of said dielectric layer and said sacrificial layer.

29. A method of forming an IC as in claim 28, wherein forming pillars in step (D) comprises the steps of:

I) depositing a conformal layer on said SOI wafer; and

II) isotropically etching said conformal layer.

30. A method of forming an IC as in claim 29, wherein said conformal layer is a nitride layer.

31. A method of forming an IC as in claim 30, wherein said sacrificial layer is a layer comprising germanium (Ge).

32. A method of forming an IC as in claim 31, wherein said sacrificial layer is a polysilicon germanium (SiGe) layer.

33. A method of forming an IC as in claim 32, wherein the step (ii) of protecting the first side comprises depositing a second SiGe layer.

34. A method of forming an IC as in claim 27, wherein said silicon layer is on a layered dielectric and the step (iv) of etching remaining portions etches through upper layers of said layer dielectric to a buried oxide layer.

35. A method of forming an IC as in claim 34, wherein said upper layers comprise an oxide layer on a nitride layer and said nitride layer is on said buried oxide layer.

36. A method of forming an IC as in claim 27, wherein the step (b) of forming back bias gates comprises:

i) forming a back bias gate dielectric layer;

ii) forming a back bias gate layer on said back bias gate dielectric layer;

iii) depositing a fill material;

iv) planarizing an upper surface of said SOI wafer; and

v) removing portions of said back bias gate layer and said back bias gate dielectric layer such that each of said pillars are exposed.

37. A method of forming an IC as in claim 36, wherein planarizing the upper surface in step (b)(iv) comprises depositing fill material and polishing with a chemical mechanical polish (CMP) to planarized said wafer.

38. A method of forming an IC as in claim 37, wherein removing portions in step (b)(v) comprises continuing CMP and stopping on said pillar.

39. A method of forming an IC as in claim 37, wherein the step (b) of forming back bias gates further comprises:

vi) forming voids between said pillars and remaining said portions of said back bias gate layer;

vii) filling said voids.

40. A method of forming an IC as in claim 36, wherein the step (c) of forming device gates comprises:

i) re-exposing said first side;

ii) forming a gate dielectric layer;

iii) forming a gate layer on said wafer;

iv) removing portions of said gate layer, device gates being separated from back bias gates and each of said pillars being exposed.

41. A method of forming an IC as in claim 40, wherein said gate dielectric layer is one fifth as thick as said back bias dielectric layer.

42. A method of forming an IC as in claim 41, wherein said gate dielectric layer is selected from a group of materials consisting of an oxide, an oxynitride and a high K dielectric.

43. A method of forming an IC as in claim 40, wherein said gate layer is the same material as said back bias gate layer.

44. A method of forming an IC as in claim 43, wherein said gate layer and said back bias gate layer are polysilicon layers.

45. A method of forming an IC as in claim 44, wherein the step (c)(ii) of forming the gate layer comprises the steps of:

A) forming polysilicon spacers on both sides of said fins, said polysilicon spacers being separated from said fins on said opposite side by said gate dielectric layer;

B) removing horizontal portions of said gate dielectric layer; and

C) depositing a polysilicon layer.

46. A method of forming an IC as in claim 45, wherein the step (c)(iv) of removing portions of the gate layer comprises the steps of:

A) directionally depositing a dielectric layer; and

B) selectively removing horizontal portions of the directionally deposited said dielectric layer, portions of said polysilicon gate layer above said pillars being exposed; and

C) isotropically etching said polysilicon gate layer.

47. A method of forming an IC as in claim 46, wherein the step (c)(iv) of forming back bias gates further comprises:

D) forming voids between said pillars and remaining said portions of said gate layer;

E) filling said voids.